What is claimed is:

1. A device comprising:

a plurality of data lines;

a memory array for storing memory data;

a conditioning data storage unit for storing conditioning data;

a data selection circuit connected to the memory array and the conditioning data storage unit for selecting data between the memory data and the conditioning data;

a data transceiver circuit connected to the data selection circuit for outputting to the data lines the data selected by the data selection circuit; and

a strobe transceiver circuit for providing timing information of the data outputted at the data lines.

2. The device of claim 1 further includes an output enable unit having a driver enable circuit connected to the strobe and data transceiver circuits for simultaneously enabling the strobe and data transceiver circuits at a first time during a memory operation.

3. The device of claim 2, wherein the output enable unit further includes a data enable circuit connected to the data selection circuit for enabling the data selection circuit to select the memory data at a second time during the memory access operation.

4. The device of claim 1, wherein the conditioning data storage unit includes multiple cells for storing multiple bits of data.

5. The device of claim 1, wherein the conditioning data storage unit includes only one cell for storing only one bit of data.

6. The device of claim 1, wherein the conditioning data storage unit is configured as a read-only storage unit.

7. A device comprising:

a plurality of data lines;

a plurality of memory cells for storing memory data;

an output data path connected to the memory cells;

a conditioning data storage unit for storing conditioning data;

a plurality of multiplexers, each of the multiplexers including a first input node connected to the output data path, a second input node connected to the conditioning data storage unit, and an multiplexing output node;

a plurality of data transceivers, each of the data transceivers connecting between the multiplexing output node and one of the data lines; and

a plurality of strobe transceivers for providing timing information of data outputted at the data lines.

8. The device of claim 7, wherein the conditioning data storage unit includes a register connected to the second input node of the multiplexer.

9. The device of claim 8, wherein the register includes a single register cell.

10. The device of claim 9, wherein the single register cell is configured to store a conditioning bit having a bit value of zero.

11. The device of claim 8, wherein the register includes multiple register cells.

12. The device of claim 7, wherein the conditioning data storage unit includes multiple register cells for storing multiple conditioning bits having multiple bit values.

13. The device of claim 12, wherein the conditioning data storage unit is configured such that the bit values of any two consecutive bits among the multiple conditioning bits are different from each other.

14. A device comprising:

a plurality of data lines;

a plurality of memory cells for storing memory data;

an output data path connected to the memory cells;

a storage node for storing conditioning data;

a plurality of multiplexers, each of the multiplexers including a first input node connected to the output data path, a second input node connected to the storage node, and an multiplexing output node;

a plurality of data transceivers, each of the data transceivers connecting between the multiplexing output node and one of the data lines; and

a plurality of strobe transceivers for providing timing information of data outputted at the data lines.

15. The device of claim 14, wherein the storage node connects to ground.

16. The device of claim 14, wherein the storage node connects to a voltage source.

17. The device of claim 14 further includes a driver enable circuit having an output node for providing a driver enable signal, wherein each of the data transceivers and each of the strobe transceivers connect to the same output node of the driver enable circuit.

18. The device of claim 17 further includes a data enable circuit having an output node for providing the data enable signal, wherein each of the multiplexers includes an enable node connected to the output node of the data enable circuit.

19. A system comprising:

a data bus;

a controller connected to the data bus; and

a memory device connected to the controller via the data bus, the memory device including:

a plurality of data lines connected to the data bus;

a memory array for storing memory data;

a conditioning data storage unit for storing conditioning data;

a data selection circuit connected to the memory array and the conditioning data storage unit for selecting data between the memory data and the conditioning data;

a data transceiver circuit connected to the data selection circuit for outputting to the data lines the data selected by the data selection circuit; and

a strobe transceiver circuit for providing timing information of the data outputted at the data lines.

20. The system of claim 19, wherein the data transceiver circuit includes a plurality of multiplexers, each of the multiplexers including a first input node connected to the memory array, a second input node connected to the conditioning data storage unit, and an multiplexing output node.

21. The system of claim 20, wherein the data transceiver circuit includes a plurality of data transceivers, each of the data transceivers connecting between the multiplexing output node and one of the data lines.

22. The system of claim 21, wherein the conditioning data storage unit includes multiple cells for storing multiple bits of data.

23. The system of claim 21, wherein the conditioning data storage unit includes only one cell for storing only one bit of data.

24. The system of claim 19, wherein the conditioning data storage unit is configured as a read-only storage unit.

25. The system of claim 19, wherein the conditioning data storage unit includes a number of register cells for storing multiple conditioning bits having multiple bit values.

26. The system of claim 25, wherein the conditioning data storage unit is configured such that the bit values of any two consecutive bits among the multiple conditioning bits are different from each other.

27. The system of claim 26, wherein the number of register cells is an odd number.

28. A method comprising:

setting a latency time interval for outputting memory data at a data line, wherein the latency time interval occurs between an issuance of a command signal and the availability of a first bit of the memory data at the data line;

outputting a conditioning data to the data line during the latency time interval; and

outputting the memory data to the data line after the latency time.

29. The method of claim 28, wherein the conditioning data includes a single conditioning bit.

30. The method of claim 29, wherein the single conditioning bit has a bit value of zero.

31. The method of claim 29, wherein the data line has an initial signal level representing a bit value before the conditioning data is transferred to the data line, wherein the single conditioning bit has a bit value, and wherein the bit value of the single conditioning bit is unequal to the bit value of the data line.

32. The method of claim 28, wherein the conditioning data includes multiple conditioning bits.

33. The method of claim 32, wherein any two consecutive bits among the number of conditioning bits have bit values different from each other.

34. The method of claim 32, wherein the number of conditioning bits is an odd number.

35. The method of claim 28, wherein outputting the conditioning data and outputting the memory data to the data line include performing a multiplexing function to select data between the conditioning data from a conditioning data storage unit and the memory data from a memory array.

36. The method of claim 28, wherein outputting the memory data includes outputting the memory data at the data line at a data rate of at least one gigabits per second.

37. A method comprising:

issuing a command signal to access memory data from a memory array;

outputting a strobe signal to a strobe line after the command signal is issued, the strobe signal having a plurality of signal transitions, wherein each of the signal transitions occurs when the strobe signal switches between a first signal level and a second signal level;

transferring a conditioning bit from a conditioning data storage unit to a data line at a first signal transition of the strobe signal after the command signal is issued; and

transferring the memory data from the memory array to the data line after the transferring of the conditioning bit.

38. The method of claim 37, wherein transferring the memory data occurs when the strobe signal has a second signal transition after the command signal is issued.

39. The method of claim 37, wherein before the conditioning bit is transferred, the data line has an initial signal level representing a bit value, and wherein the conditioning bit has a bit value unequal to the bit value of the data line.

40. The method of claim 37, wherein the conditioning bit has a bit value of zero.

41. A method comprising:

issuing a command signal;

providing a strobe signal to a strobe line after the command signal is issued, the strobe signal having a plurality of signal transitions, wherein each of the signal transition occurs when the strobe signal switches between a first signal level and second signal level;

transferring a conditioning data from a conditioning data storage unit to a data line during a conditioning time interval after the command signal is issued; and

transferring a memory data from a memory array to the data line after the conditioning time interval.

42. The method of claim 41, wherein transferring the conditioning data occurs when the strobe signal has a first signal transition after the command signal is issued.

43. The method of claim 42, wherein the conditioning data includes a single conditioning bit.

44. The method of claim 43, wherein the single conditioning bit has a bit value of zero.

45. The method of claim 41, wherein the strobe signal has at least one signal transition during the conditioning time interval.

46. The method of claim 45, wherein transferring the conditioning data includes transferring a number of conditioning bits.

47. The method of claim 46, wherein at least two of the conditioning bits have bit values different from each other.

48. The method of claim 46, wherein the number of conditioning bits equals a number of signal transitions of the strobe signal during the conditioning time interval.

49. The method of claim 46, wherein transferring the number of conditioning bits includes transferring one of the conditioning bits when the strobe signal has a first signal transition after the command signal is issued.

50. The method of claim 41, wherein the command signal is a read command signal for reading data from the memory array.

51. A method comprising:

issuing a command signal;

simultaneously enabling a strobe transceiver and a data transceiver during a conditioning time interval after the command signal is issued;

outputting a strobe signal from the strobe transceiver to a strobe line;

transferring a conditioning data from a conditioning data storage unit to the data transceiver based on a first state of a data enable signal;

outputting the conditioning data from the data transceiver to a data line during the conditioning time interval;

transferring a memory data from a memory array to the data transceiver based on a second state of the data enable signal; and

outputting the memory data from the data transceiver to the data line after the conditioning time interval.

52. The method of claim 51, wherein transferring the conditioning data and transferring the memory data to the data transceiver include performing a multiplexing function to select data between the conditioning data and the memory data.

53. The method of claim 51, wherein the conditioning data includes a single conditioning bit.

54. The method of claim 53, wherein the single conditioning has a bit value of zero.

55. The method of claim 51, wherein the conditioning data includes multiple conditioning bits.

56. The method of claim 55, wherein a first conditioning bit of the multiple conditioning bits has a first bit value and a second conditioning bit of the multiple conditioning bits has a second bit value.